Amendments To The Claims

Please cancel claim 4 without prejudice or disclaimer.

1. (Currently Amended) A semiconductor device comprising:

a substrate;

a source/drain diffused layer formed in the substrate for a transistor;

a first shallow trench isolation formed in the substrate;

a second shallow trench isolation formed in the substrate; and

a dummy diffused layer formed ~~in the substrate~~ between the first and second shallow trench isolations,[[; and]]

~~a shallow trench isolation formed between the source/drain diffused layer and the dummy diffused layer,~~

wherein the source/drain diffused layer has its surface silicided, and

wherein the dummy diffused layer has its surface covered with an anti-silicidation film at least partially, on which no gate electrode is provided.

2. (Original) The device of Claim 1, wherein the anti-silicidation film is an oxide film.

3. (Original) The device of Claim 1, wherein a dopant, which has been introduced into the source/drain diffused layer, has not been introduced into the dummy diffused layer.

Claim 4 (Cancelled)

5. (Previously Presented) A semiconductor device comprising:

a substrate;

a source/drain diffused layer formed in the substrate for a transistor; and

a dummy diffused layer formed in the substrate,

wherein the source/drain diffused layer has its surface silicided,

wherein the dummy diffused layer has its surface covered with a dummy gate electrode at least partially,

wherein the dummy diffused layer is located between a circuit block and another circuit block, and

wherein the dummy gate electrode is divided into at least two portions disposed between the two circuit blocks.

6. (Previously Presented) A semiconductor device comprising:

a substrate;

a source/drain diffused layer formed in the substrate for a transistor; and

a dummy diffused layer formed in the substrate,

wherein the source/drain diffused layer has its surface silicided,

wherein the dummy diffused layer has its surface covered with a dummy gate electrode at least partially, and

wherein the dummy gate electrode has a fixed potential level.

7. (Previously Presented) The device of Claim 5, wherein a dopant, which has been introduced into the source/drain diffused layer, has not been introduced into the dummy diffused layer.

8. (Original) A semiconductor device comprising:

a substrate;

a source/drain diffused layer formed in the substrate for a transistor; and

a dummy diffused layer formed in the substrate,

wherein the source/drain and dummy diffused layers have their surfaces silicided, ~~and~~

wherein a well of a first conductivity type is defined in the substrate, and

wherein the dummy diffused layer is formed in the well and a dopant of a second conductivity type has been introduced into the dummy diffused layer, the second conductivity type being opposite to the first conductivity type.

9. (Original) The device of Claim 8, wherein the dummy diffused layer has a fixed potential level.

10. (Original) The device of Claim 9, wherein the potential level of the dummy diffused layer is fixed at such a level as applying a reverse bias to a pn junction diode formed by the dummy diffused layer and the well.

11. (Original) The device of Claim 9, wherein the dummy diffused layer is divided into multiple portions, and

wherein the portions of the dummy diffused layer are connected together by silicide diffused layer interconnects that have been formed in the same layer as the dummy diffused layer.

12. (Original) A semiconductor device comprising:

a substrate of a first conductivity type;

a source/drain diffused layer, which is formed in the substrate for a transistor and has its surface silicided;

a first well of a second conductivity type, the first well being defined in the substrate, the second conductivity type being opposite to the first conductivity type;

a dummy diffused layer formed in the first well and located between two circuit blocks; and

a second well of the first conductivity type, the second well being defined between the first well and one of the two circuit blocks.

13. (Original) The device of Claim 12, wherein potential levels of the first and second wells are fixed at such levels as applying a reverse bias to a pn junction diode formed by the first and second wells.

14. (Previously Presented) The semiconductor device of claim 1,

wherein the dummy diffused layer is located between an analog circuit block and a digital circuit block.

15. (Previously Presented) The semiconductor device of claim 1,

wherein the dummy diffused layer is not electrically coupled to another component via an interconnect.

16. (Previously Presented) A semiconductor device comprising:

a substrate;

a source/drain diffused layer formed in the substrate for a transistor; and

a dummy diffused layer formed in the substrate,

wherein the source/drain diffused layer has its surface silicided,

wherein the dummy diffused layer has its surface covered with a dummy gate electrode at least partially, and

wherein the dummy diffused layer is located between a digital circuit block and an analog circuit block.

17. (Previously Presented) The device of claim 5, wherein the dummy diffused layer is not electrically coupled to another component via an interconnect.

18. (New) The device of Claim 1,

wherein the dummy diffused layer is formed so as to prevent dishing.

19. (New) The device of Claim 1,

wherein no transistor is formed between the first shallow trench isolation and the second shallow trench isolation.